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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,649	04/14/2004	Takashi Kurihara	1076.1094	4917

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/823,649	KURIHARA ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,21 and 24* is/are pending in the application.

4a) Of the above claim(s) *12-20,22,23, and 25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,21 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is response to Application Amendment filed on 07/16/2007. Claims 1-11, 21, and 24 remain pending in this instance office action. Claims 1, 11, 21, and 24 have been amended. Claims 16-19 have been canceled.

Response to Arguments

2. Applicant's arguments with respect to claims 1,11, 21, and 24 have been considered but are moot in view of the new ground(s) of rejection and the allowance subject matter on the last office action is withdrawn as new found reference (see the claim rejection).

Examiner Remarks

3. Claims 12-15, 20, 22, 23, and 25 have been withdraw from consideration. However, Applicant(s) is/are informed to cancel these claims 12-15, 20, 22, 23, and 25, which are non-elected claimed in the next communication.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method and Apparatus Distribution Power Supply Pad of Semiconductor Integrated Circuit.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-11, 21, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable by Tuan et al., (US Patent 6,311,147) in view of Ito (US Patent 5,946,477) (see entire documents).

7. With respect to claims 1, 7, 9-11, 21, and 24, Tuan teach a method of power analysis of integrated circuit (IC) to determine current value for IC devices at specify supply voltage ('147, the abstract) comprises:

(claim 21) storage device which stores power consumption information of the core section and power supply wire resistance information, including resistances between the nodes ('147, figs. 1-3 see the descriptions);

(claim 21) a data processor in communication with the storage device, in which the data processor ('147, figs. 1-3);

(claims 1, 11, 21, and 24) Performing a power supply network analysis of the core section based on power consumption information of the core section (transistor network) ('147, fig. 4 and col. 2, ll. 30-37) and power supply wire resistance information, which includes resistances between the nodes ('147, fig. 4, fig. 7, fig. 13, steps [1302] [1310], col. 2, ll. 34-43, col. 9, ll. 8-43), to calculate voltage values of the nodes (fig. 9, col. 9, line 44 – col. 10, line 8); (claims 7 and 9) power supply pads having the potential as the same (e.g., Vdd) ('147, figs. 4, 7, and 9, col. 9, ll. 29-32);

(claims 1, 11, 21, and 24) calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes ('147, fig. 9, col. 9, ll. 44-63 and col. 10, ll. 13-19);

(claims 1, 11, 21, and 24) calculating current values of the power supply pads from the current values between the nodes ('147, col. 2, ll. 37-40, fig. 9, step [914], col. 10, ll. 16-18);

(claims 1, 11, 21, and 24) determining (checking) current density value of each of the power supply pads whether exceed or greater than threshold ('147, fig. 12 and fig. 13, col. 11, line 20 – col. 12, line 20) for determining characteristic of portion the power net ('147, col. 2, ll. 37-42) which includes a power pad and metal lines (net) connected power pad and transistor network. The metal lines in the power net typically act as small resistors (IO buffer) that lower the voltage applied to the transistor network ('147, fig. 4, col. 5, ll. 45-56, col. 11, ll. 42-52). Tuan also teaches the step updating the resistors of metal net if the current density is exceed the current Global Maximum Current Density Value (threshold), which defined in configuration filed ('147, col. 11, ll. 43-60).

However, Tuan does not implicitly teach the step (claims 1, 7, 9-11, 21, and 24) eliminating or adding (modifying) at least one power supply pad with respect to the result of the determination.

Ito teaches a method for provisionally determining quantity and positions of a plurality of power supply pads when designing a semiconductor integrated circuit ('477, the abstract, col. 3, ll. 40-60) including a core section (internal circuit) provided with a plurality of nodes (terminal pad) and the plurality of power supply pads (power supply test pads or terminal), with each power supply pad being connected to the core section via an IO buffer ('477, the abstract, col. 3, ll. 40 –60, col. 4, ll. 27-39). Ito also teaches method of rearrangement power pad by performing insertion/positioning of at least a

pair power supply test pads or the pair of test pads and chip terminals which are connected to the pair of power supply lines in each of the plurality of groups in the form of rows by performing layout position adjustment of the input/output buffers and when a length of one of the rows of the input/output buffer exceeds a length of one side of the semiconductor chip upon the insertion/positioning ('477, col. 4, ll. 27-39, col. 8, ll. 53-59), (claims 9 and 10) the number and position of power supply pads/terminals are inserted in each row of input/output buffers as reference pad (col. 9, ll. 1-12 and ll. 34-37 and col. 10, ll. 1-26) and (claim 11) each positioning/wiring are designation (assigning) as different size/type of input/output buffer and/or power supply terminal/pad which sufficient to the internal block (core) circuit ('477, col. 11, ll. 7 – 65 and col. 13, ll. 4-55). It would have been obvious to one of ordinary skill in the art the length of input/output buffer is one of critical parameters respectively to the current density and voltage drop checking in the power network analysis in Tuan's invention.

It would have been obvious to one of ordinary skill in the art at the time of invention is made to combine Ito and Tuan teaching to improve input/output buffer and/or chip terminal arrangement in entire semiconductor chip region at a high density that reduce unbalance between number of input/output buffer and chip internal circuit and also reduces cost of chip manufactured ('477, col. 5, ll. 6-11 and col. 5, ll. 35-60).

8. With respect to claim 2, Tuan and Ito teach the method according to claim 1, wherein said calculating voltage values of the nodes includes calculating IR drop values between the nodes based on the voltage value each node and suspending subsequent

processing when any one of the calculated IR drop values exceeds a predetermined maximum IR drop value ('147, figs. 10 and 11, col. 10, lines 19 – col. 11, line 19).

9. With respect to claim 3, Tuan and Ito teach the method according to claim wherein said performing a power supply network analysis includes modeling the core section as a plurality of equivalent circuits electrically equivalent to one another, each equivalent circuit including a resistor and a current source and performing the power supply network analysis on the modeled core section ('147, figs. 1-5A, figs. 7-9, see the descriptions).

10. With respect to claim 4, Tuan and Ito teach the method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of power supply wire density the core section ('147, the abstract, and figs. 4, 5A, and 7, see the descriptions; '477, fig. 4, col. 7, ll. 8-28).

11. With respect to claim 5, Tuan and Ito teach the method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of power consumption of the core section ('147, the abstract, and figs. 4, 5A, and 7, see the descriptions; '477, fig. 4, col. 7, ll. 8-28).

12. With respect to claim 6, Tuan and Ito teach the method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of the current values of the power supply pads ('147, the abstract, and figs. 4, 5A, 7, fig. 9, see the descriptions).

13. With respect to claim 8, Tuan and Ito teach the method according to claim 7, further comprising: determining whether a completion condition is satisfied after deleting

the at least one power supply pad, wherein subsequent processing is terminated when the completion condition is satisfied, and said performing a power supply network analysis is executed again when the completion condition is not satisfied ('147, fig. 11 and fig. 13, with descriptions).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for unpublished applications is available through Private PAIR only. If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nghia M. Doan
/NMD/

JACK CHIANG
SUPERVISORY PATENT EXAMINER